

SELF-OSCILLATING HALF-BRIDGE DRIVER

1. Description

The iT6800 are Half-Bridge gate driver ICs, and incorporates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS555 timer. The iT6800 provides more functionality and is easier to use. A shutdown feature has been designed into the C_T pin, so that both gate driver outputs can be disabled using a low voltage control signal. In addition, the gate driver output pulse widths are the same once the rising under voltage lockout threshold on V_{CC} has been reached, resulting in a more stable profile of frequency vs. time at startup. Noise immunity has been improved significantly, both by lowering the peak di / dt of the gate drivers, and by increasing the under voltage lockout hysteresis to 1 V. Finally, special attention has been paid to maximizing the latch immunity of the device, and providing comprehensive ESD protection on all pins.

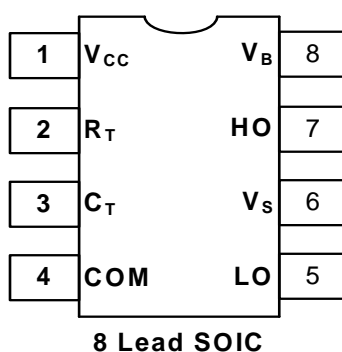
2. Features

- Integrated 600 V half-bridge gate driver
- True micro-power start up
- Low temperature coefficient dead-time
- Shutdown feature(1 / 6th V_{CC}) on C_T pin
- Increased under-voltage lockout Hysteresis(1 V)
- Lower power level-shifting circuit
- Constant LO, HO pulse widths at startup
- Lower di / dt gate driver for better noise immunity
- Low side output in phase with R_T
- Excellent latch immunity on all inputs and outputs
- ESD protection on all leads
- Also available LEAD-FREE

3. Applications

Ballast

4. Pin Assignments



5. Marking information

Product Name	Marking
iT6800	<div style="display: inline-block; border: 1px solid black; padding: 2px;">iT6800 XXXXX</div> X : Date Code

6. Ordering Code

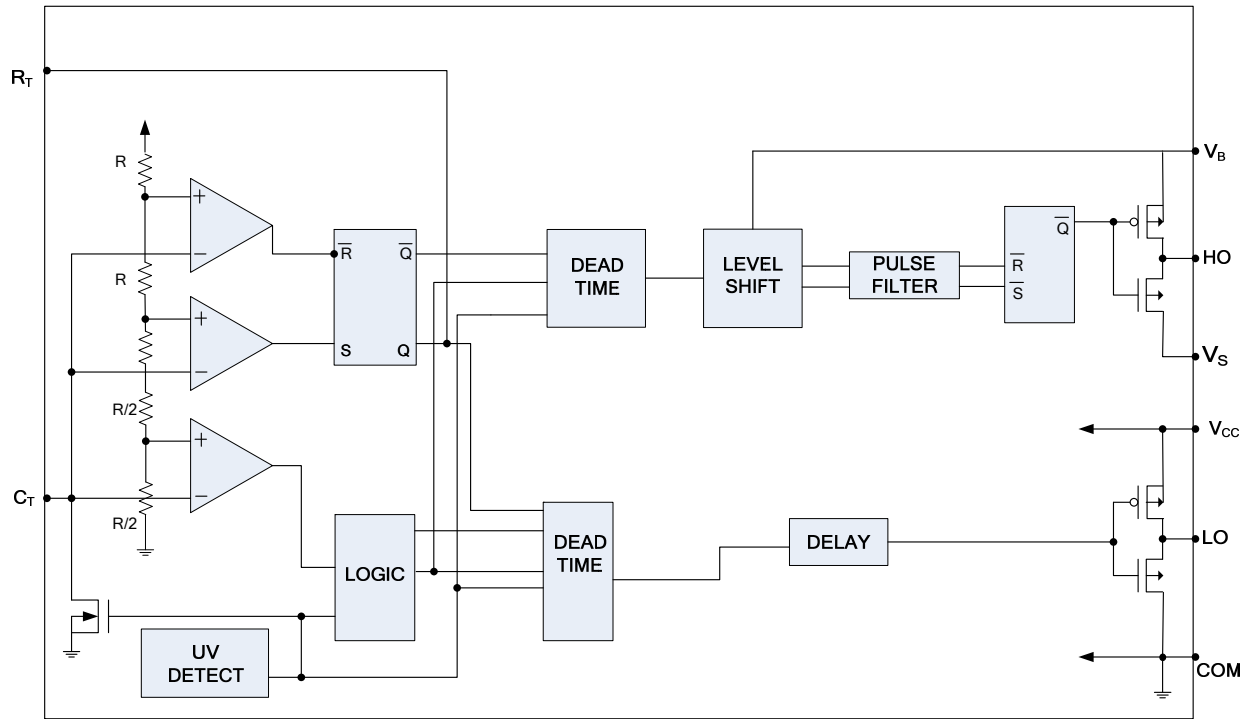
iT6800 □ └─ Assembly Material	Assembly Material G: Halogen and Lead Free Device
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Note: inergy defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

7. Pin Definitions

Pin No.	Symbol	Description
1	V_{CC}	Logic and internal gate drive supply voltage
2	R_T	Oscillator timing resistor input
3	C_T	Oscillator timing capacitor input
4	COM	IC power and signal ground
5	LO	Low side gate driver output
6	V_S	High voltage floating supply return
7	HO	High side gate driver output
8	V_B	High side gate driver floating supply

8. Block Diagram



9. Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits and beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	618	V
V_S	High side floating supply offset voltage	$V_B - 18$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{LO}	Low side output voltage	- 0.3	$V_{CC} + 0.3$	
V_{RT}	R_T pin voltage	- 0.3	$V_{CC} + 0.3$	
V_{CT}	C_T pin voltage	- 0.3	$V_{CC} + 0.3$	
I_{CC}	Supply current (note 1)	-	20	mA
I_{RT}	R_T pin current	- 5	5	
dV / dt	Allowable offset voltage slew rate	- 50	50	V / ns
P_D	Maximum power dissipation @ $T_A \leq + 25^\circ\text{C}$ (8 lead SOIC)	-	0.625	W
R_{thJA}	Thermal resistance, junction to ambient (8 lead SOIC)	-	200	$^\circ\text{C} / \text{W}$
T_J	Junction temperature	- 55	150	$^\circ\text{C}$
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

Note : This supply pin should not be driven by a DC, which is low impedance power source greater than the V_{CLAMP} .

10. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{BS}	High side floating supply voltage	$V_{CC} - 0.7$	18	V
V_S	Steady state high side floating supply offset voltage	- 3.0 (note 2)	600	
V_{CC}	Supply voltage	10	18	
I_{CC}	Supply current	(note 3)	5	mA
T_J	Junction temperature	- 40	125	$^\circ\text{C}$

Note 1 : This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} SPECIFIED IN THE Electrical Characteristics section.

Note 2 : Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5V.

Note 3 : Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

11. Static Electrical Characteristics

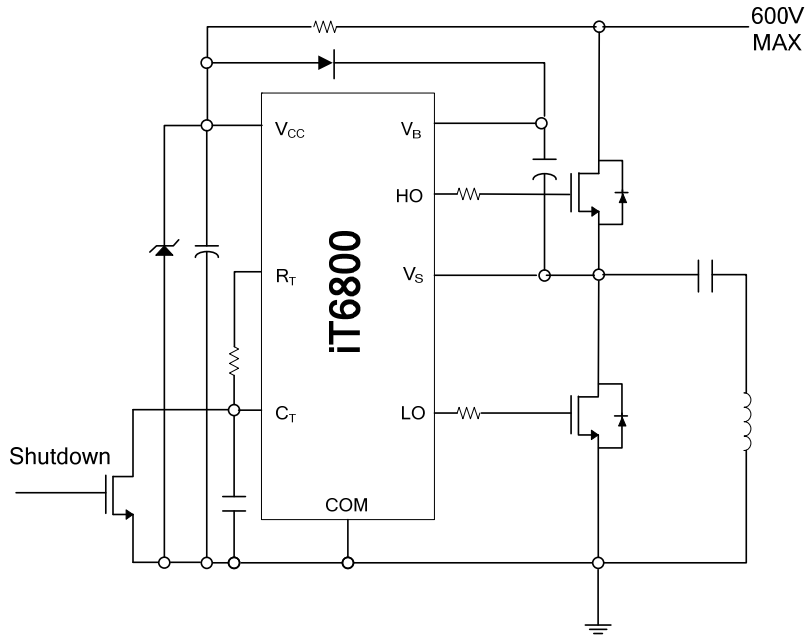
$V_{BIAS} (V_{CC}, V_{BS}) = 12\text{ V}$, $C_T = 1\text{ nF}$, $V_S = 0\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to COM and are applicable to the respective output leads : HO or LO.
 $C_{LO} = C_{HO} = 1\text{ nF}$.

Symbol	Definition	Min	Typ	Max	Unit	Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} under-voltage lockout threshold	-	11.4	-	V	
V_{CCUV-}	Falling V_{CC} under-voltage lockout threshold	-	9.8	-		
$V_{CCUVHYS}$	V_{CC} under-voltage lockout Hysteresis	-	1.6	-		
I_{QCCUV}	Micro-power startup V_{CC} supply current	-	103	-	μA	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	-	400	-		$V_{CC} \geq V_{CCUV+}$
Floating Supply Characteristics						
I_{QBS}	Quiescent V_{BS} supply current	-	20	-	μA	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold	-	6.5	-	V	
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold	-	5.5	-		
I_{LK}	Offset supply leakage current	-	-	50	μA	$V_B = V_S = 600\text{ V}$
Oscillator I / O Characteristics						
f_{OSC}	Oscillator frequency	-	18.24	-	kHz	$R_T = 36\text{ K}$
		88	93	100		$R_T = 6.2\text{ K}$
d	R_T pin duty cycle	-	50	-	%	$f_{OSC} < 100\text{ kHz}$
I_{CT}	C_T pin current	-	0.02	1	μA	
I_{CTUV}	UV-mode C_T ramp voltage threshold	-	0.70	1.2	mA	$V_{CC} = 7\text{ V}$
V_{CT+}	Upper C_T ramp voltage threshold	-	8.2	-	V	
V_{CT-}	Lower C_T ramp voltage threshold	-	3.86	-		
V_{CTSD}	C_T voltage shutdown threshold	-	1.9	-		
V_{RT+}	High-level R_T output voltage, $V_{CC} - V_{RT}$	-	10	50	mV	$I_{RT} = -100\text{ }\mu\text{A}$
		-	100	300		$I_{RT} = -1\text{ mA}$
V_{RT-}	Low-level R_T output voltage	-	10	50		$I_{RT} = 100\text{ }\mu\text{A}$
		-	100	300		$I_{RT} = 1\text{ mA}$
V_{RTUV}	UV-mode R_T ramp voltage	-	0	100		$V_{CC} \leq V_{CCUV-}$
V_{RTSD}	SD-mode R_T ramp voltage, $V_{CC} - V_{RT}$	-	10	50		$I_{RT} = -100\text{ }\mu\text{A}$, $V_{CT} = 0\text{ V}$
		-	100	300		$I_{RT} = -1\text{ mA}$, $V_{CT} = 0\text{ V}$

11. Static Electrical Characteristics (cont.)

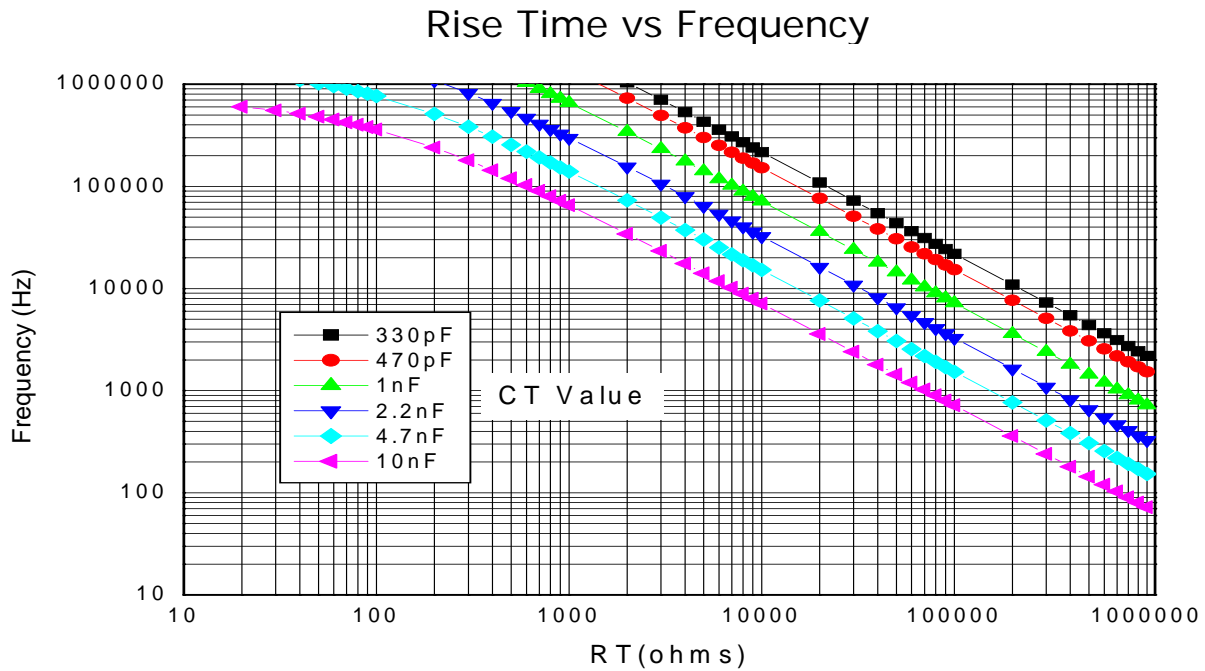
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{RTUV}	UV-mode R_T output voltage	$V_{CC} \leq V_{CCUV-}$	-	0	-	mV
V_{RTSD}	SD-Mode R_T output voltage, $V_{CC} - V_{RT}$	$I_{RT} = 100 \mu A, V_{CT} = 0V$	-	10	-	
		$I_{RT} = 1 mA, V_{CT} = 0V$	-	10	-	
Gate Driver Output Characteristics						
V_{OH}	High-level output voltage, $V_{BIAS} - V_O$	$I_O = 0 A$	-	0	-	mV
V_{OL}	Low-level output voltage, V_O	$I_O = 0 A$	-	0	-	
V_{OL_UV}	UV-mode output voltage, V_O	$I_O = 0 A$ $V_{CC} \leq V_{CCUV-}$	-	0	-	
t_r	Output rise time		-	80	-	nsec
t_f	Output fall time		-	45	-	
t_{sd}	Shutdown propagation delay		-	660	-	
t_d	Output dead-time (HO or LO)		-	1.20	-	
						μsec

12. Application Circuit



13. Recommended Component Values

Symbol	Conditions	Min	Max	Unit
R_T	Timing resistor value	10	-	k Ω
C_T	C_T pin capacitor value	330	-	pF



14. Timing Diagram

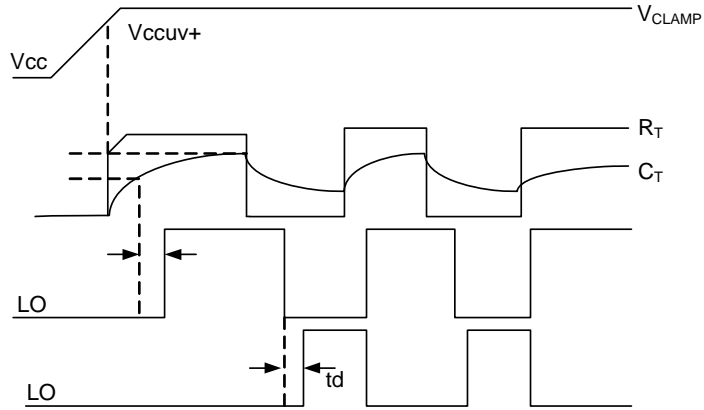


Figure 1. Input / Output Timing Diagram

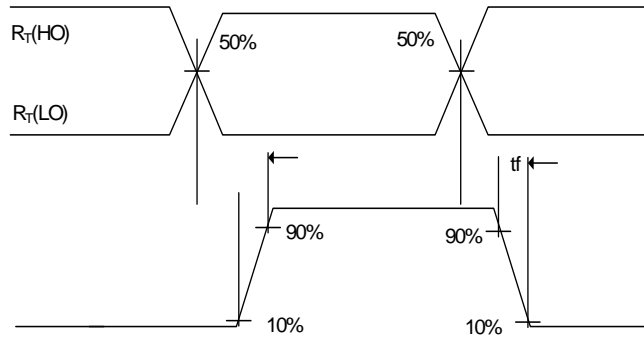


Figure 2. Switching Time Waveform

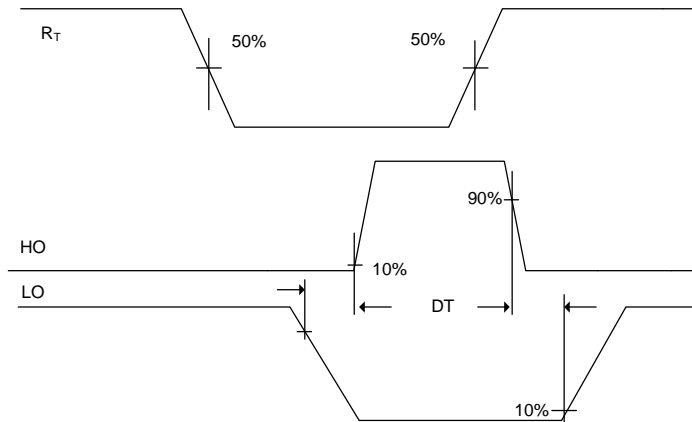
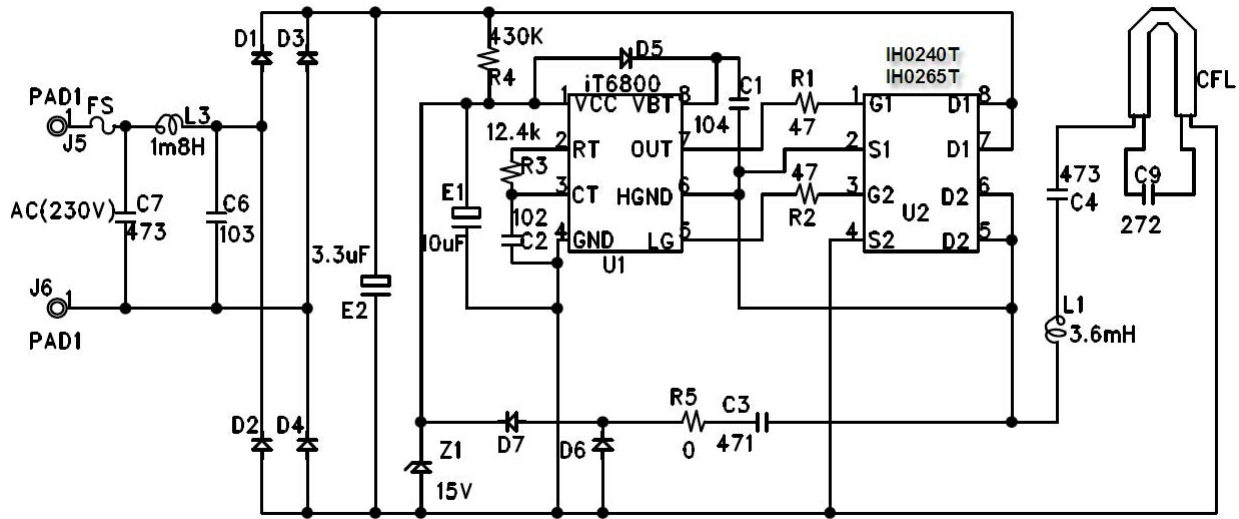


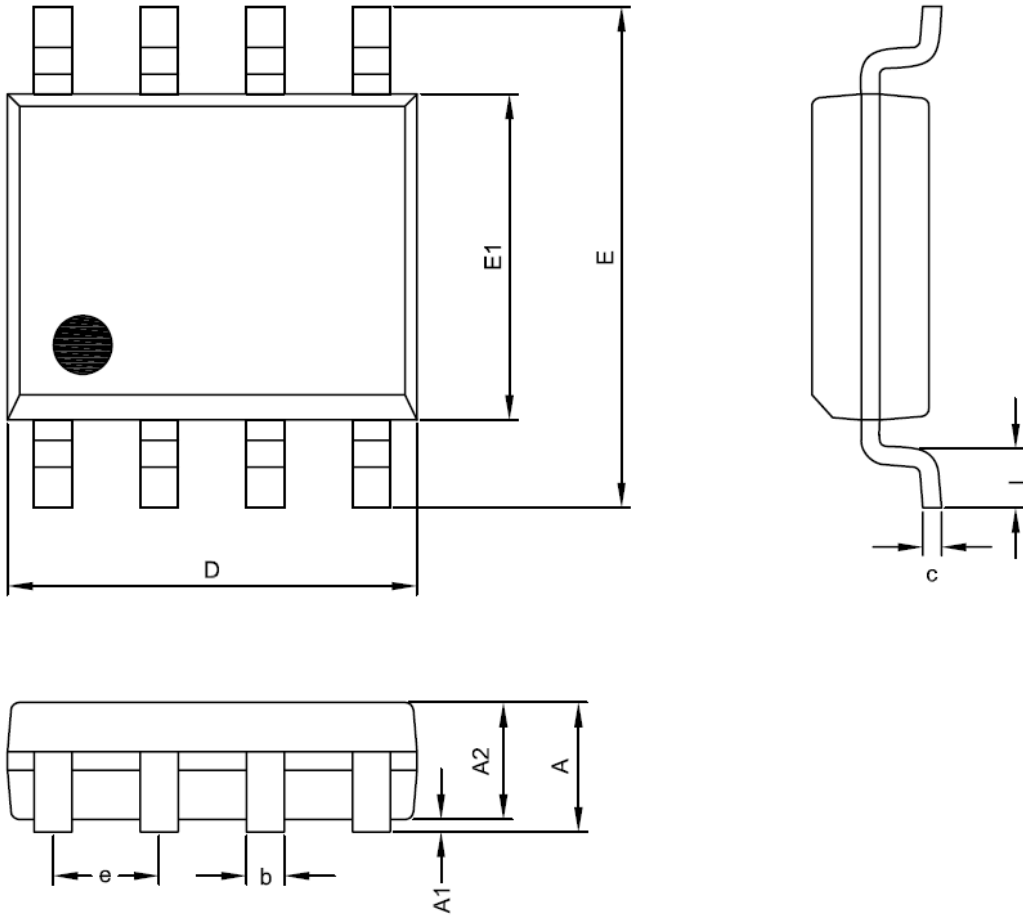
Figure 3. Dead-Time Waveform Definitions

15. Application Information



16. Package Dimensions

SOP- 8



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.