



**HIGH EFFICIENCY 200KHz 5A SYNCHRONOUS AND  
ASYNCHRONOUS PWM CONVERTER**

**FEATURES**

- Synchronous Converter with Low side MOSFET Driver
- Operating with single 5V or 12V supply voltage
- Internal 200KHz Oscillator
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability in Low side MOSFET Driver
- Protects the output when control FET is shorted
- APU1855 has 5A output current
- RoHS Compliant

**APPLICATIONS**

- DDR memory source sink Vt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

**DESCRIPTION**

The APU1855 converter IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter applications. With the migration of today's ASIC products requiring low supply voltages such as 1.8V and lower, together with currents in excess of 5A, traditional linear regulators are simply too lossy to be used when input supply is 5V or even in some cases with 3.3V input supply. The APU1855 with built-in High side N-channel MOSFETs, provide a low cost solution for such applications. This device features an internal 200KHz oscillator, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

**TYPICAL APPLICATION**

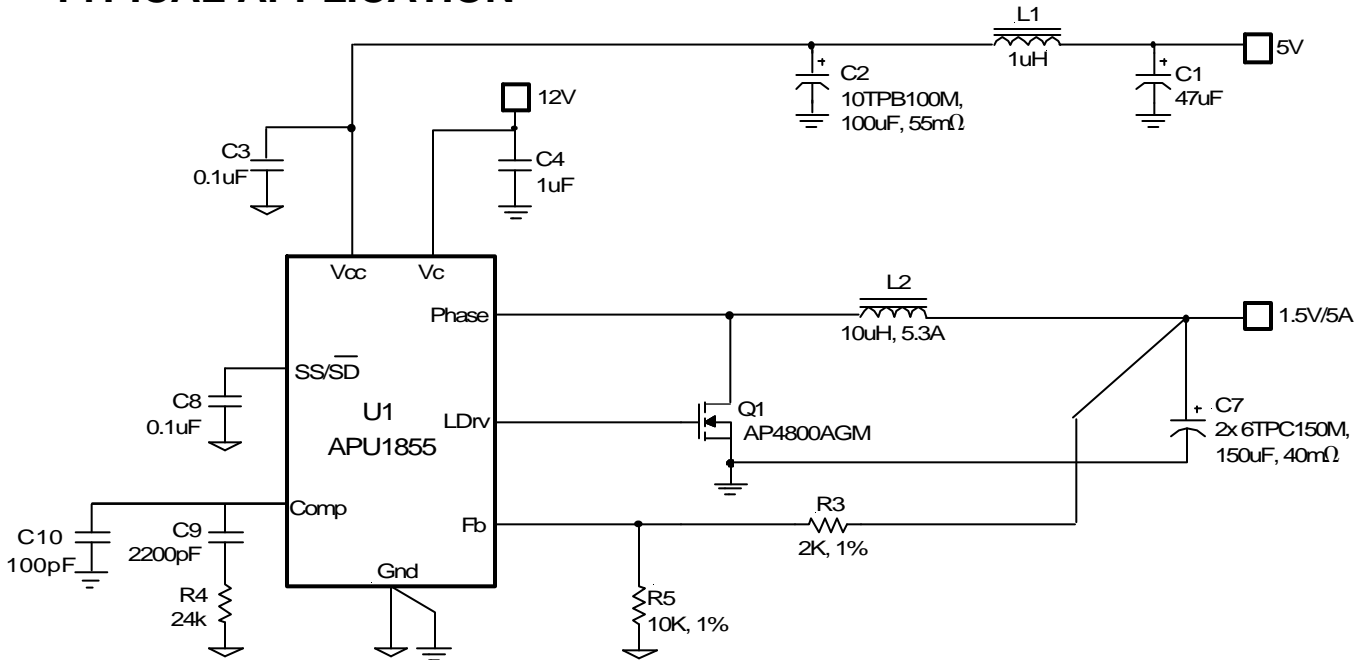


Figure 1 - Typical application of APU1855

**PACKAGE ORDER INFORMATION**

T <sub>A</sub> (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	APU1855M	8-Pin Plastic SOP (M)	200KHz

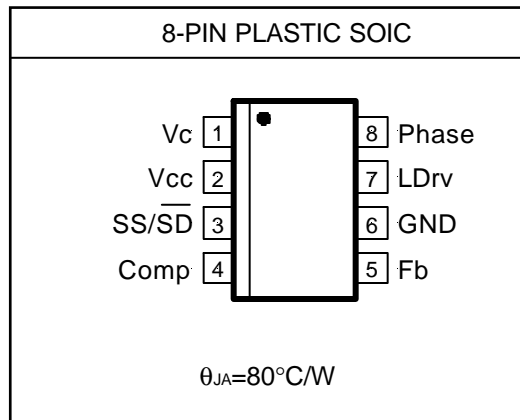


## ABSOLUTE MAXIMUM RATINGS

V <sub>cc</sub> Supply Voltage .....	20V
V <sub>c</sub> Supply Voltage .....	30V (not rated for inductive load)
Storage Temperature Range .....	-65°C To 150°C
Operating Junction Temperature Range .....	0°C To 125°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

## PACKAGE INFORMATION



## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V<sub>cc</sub>=5V, V<sub>c</sub>=12V and T<sub>A</sub>=0 to 70°C. Typical values refer to T<sub>A</sub>=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
<b>Reference Voltage</b>						
Fb Voltage	V <sub>FB</sub>	APU1855	1.225	1.250	1.275	V
Fb Voltage Line Regulation	L <sub>REG</sub>	5<V <sub>cc</sub> <12		0.2	0.35	%
<b>UVLO</b>						
UVLO Threshold - V <sub>cc</sub>	UVLO V <sub>CC</sub>	Supply Ramping Up	4.0	4.2	4.4	V
UVLO Hysteresis - V <sub>cc</sub>				0.25		V
UVLO Threshold - V <sub>c</sub>	UVLO V <sub>C</sub>	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - V <sub>c</sub>				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.4	0.6	0.8	V
UVLO Hysteresis - Fb				0.1		V
<b>Supply Current</b>						
V <sub>cc</sub> Dynamic Supply Current	Dyn I <sub>CC</sub>	Freq=200KHz, C <sub>L</sub> =1500pF	2	5	8	mA
V <sub>c</sub> Dynamic Supply Current	Dyn I <sub>C</sub>		2	7	10	mA
V <sub>cc</sub> Static Supply Current	I <sub>CCQ</sub>	SS=0V	1	3.3	6	mA
V <sub>c</sub> Static Supply Current	I <sub>CQ</sub>	SS=0V	0.5	1	4.5	mA
<b>Soft-Start Section</b>						
Charge Current	SS <sub>IB</sub>	SS=0V	-10	-20	-30	μA



PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
<b>Error Amp</b>						
Fb Voltage Input Bias Current	I <sub>FB1</sub>	SS=3V, Fb=1V		-0.1		μA
Fb Voltage Input Bias Current	I <sub>FB2</sub>	SS=0V, Fb=1V		-64		μA
Transconductance	gm		450	600	750	μmho
<b>Oscillator</b>						
Frequency	Freq	APU1855	180	200	220	KHz
Ramp-Amplitude Voltage	V <sub>RAMP</sub>		1.225	1.25	1.275	V
R <sub>DS(ON)</sub>	R <sub>DS</sub>	VGS=10V/APU1855 VGS=4.5V/APU1855		25 40		mohm
Max Output Current	I <sub>OUT</sub>		5.0		5.5	A
<b>Output Drivers</b>						
Dead Band Time	T <sub>DB</sub>		50	150	250	ns
Max Duty Cycle	T <sub>ON</sub>	Fb=1V, Freq=200KHz	85	90	95	%
Min Duty Cycle	T <sub>OFF</sub>	Fb=1.5V	0	0		%

## PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V <sub>c</sub>	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
2	V <sub>cc</sub>	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
3	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.
4	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
5	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
6	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from V5 and V12 pins to this pin for noise free operation.
7	LD <sub>rv</sub>	Output driver for the synchronous power MOSFET.
8	Phase	This Pin is power switch must be connected external inductor and Drain of the Low side MOSFET.

**BLOCK DIAGRAM**

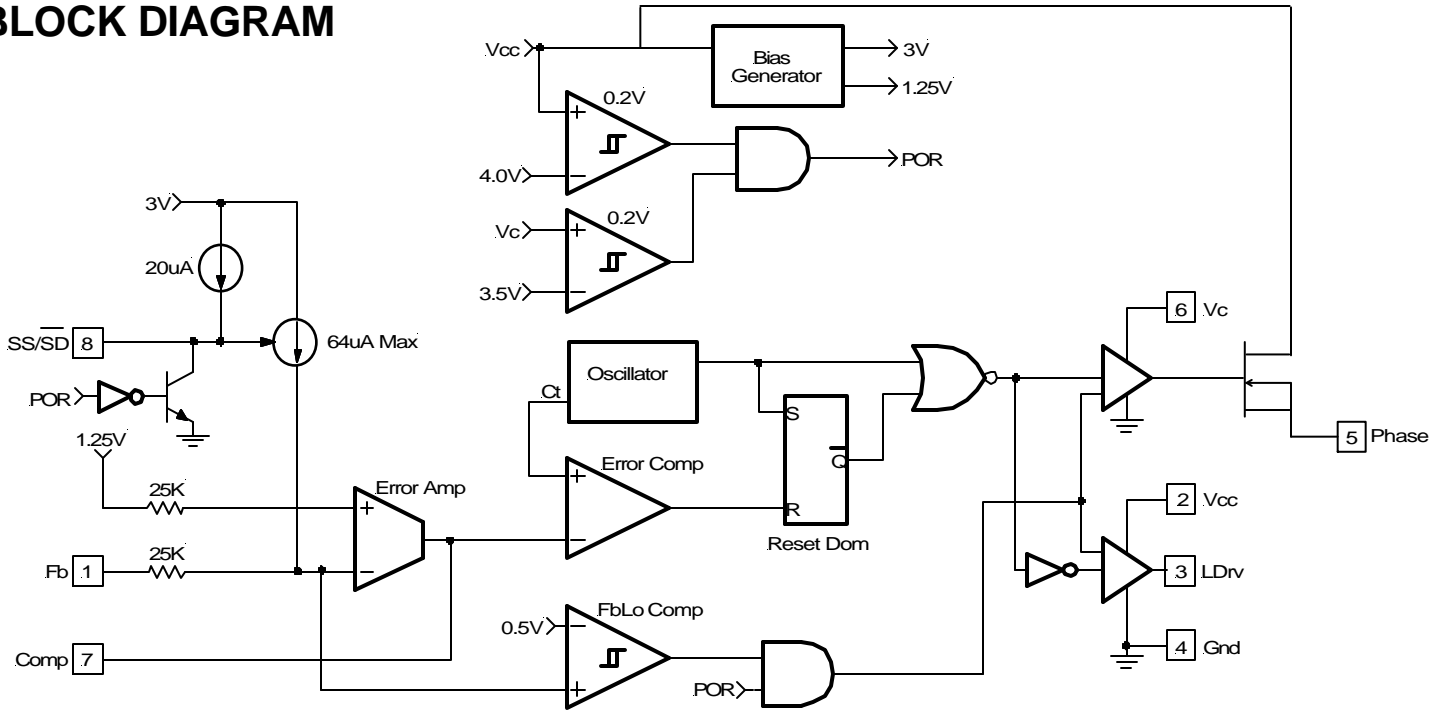


Figure 2 - Simplified block diagram of the APU1855.

**THEORY OF OPERATION**

**Introduction**

The APU1855 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, low side 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which low side drives the N-channel external MOSFETs. The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 200 KHz.

**Soft-Start**

The APU1855 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates

the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

**Short-Circuit Protection**

The outputs are protected against the short-circuit. The APU1855 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The APU1855 shuts down the PWM signals, when the output voltage drops below 0.6V.

The APU1855 also protects the output from over-volting when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

**Under-Voltage Lockout**

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.



## APPLICATION INFORMATION

### Design Example:

The following example is a typical application for APU1855, the schematic is Figure 12 on page 12.

$$\begin{aligned} V_{IN} &= 5V \\ V_{OUT} &= 3.3V \\ I_{OUT} &= 5A \\ \Delta V_{OUT} &= 100mV \\ f_s &= 200KHz \end{aligned}$$

### Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R_6}{R_5} \right) \quad \text{---(1)}$$

When an external resistor divider is connected to the output as shown in Figure 3.

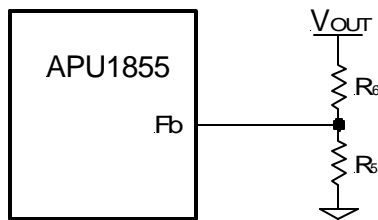


Figure 3 - Typical application of the APU1855 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left( \frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Choose  $R_5 = 1K\Omega$

This will result to  $R_6 = 1.65K\Omega$

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

### Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times C_{SS} \quad (ms) \quad \text{---(2)}$$

Where:

$C_{SS}$  is the soft-start capacitor ( $\mu F$ )

For a start-up time of 7.5ms, the soft-start capacitor will be  $0.1\mu F$ . Choose a ceramic capacitor at  $0.1\mu F$ .

### Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.5V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

### Boost Supply Vc

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 18. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of  $0.1\mu F$  to  $1\mu F$  is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in Figure 1.

### Input Capacitor Selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power-up. The APU1855 provides the soft-start function which controls and limits the current surge. The value of the input capacitor can be calculated by the following formula:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \quad \text{---(3)}$$

Where:

$C_{IN}$  is the input capacitance ( $\mu F$ )

$I_{IN}$  is the input current (A)

$\Delta t$  is the turn on time of the high-side switch ( $\mu s$ )

$\Delta V$  is the allowable peak to peak voltage ripple (V)



Assuming the following:

$$\Delta V = 1\%(V_{IN}), \text{ Efficiency}(\eta) = 90\%$$

$$\Delta t = D \times \frac{1}{f_s} \rightarrow \Delta t = 3.3\mu s$$

$$I_{IN} = \frac{V_o \times I_o}{\eta \times V_{IN}} \rightarrow I_{IN} = 5.56A$$

By using equation (3),  $C_{IN} = 183.3\mu F$   
 For higher efficiency, low ESR capacitor is recommended.  
 Choose two 100 $\mu F$  capacitors.

The Sanyo TPB series PosCap capacitor 100 $\mu F$ , 10V with 55m $\Omega$  ESR is a good choice.

### Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_o}{\Delta I_o} \quad \text{---(4)}$$

Where:

$\Delta V_o$  = Output Voltage Ripple

$\Delta I_o$  = Output Current

$\Delta V_o=100mV$  and  $\Delta I_o=5A$

Results to  $ESR=33m\Omega$

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC220M 220 $\mu F$ , 6.3V has an ESR 30m $\Omega$ . which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

### Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor ( $\Delta i$ ). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} ; \Delta t = D \times \frac{1}{f_s} ; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_s} \quad \text{---(5)}$$

Where:

$V_{IN}$  = Maximum Input Voltage

$V_{OUT}$  = Output Voltage

$\Delta i$  = Inductor Ripple Current

$f_s$  = Switching Frequency

$\Delta t$  = Turn On Time

$D$  = Duty Cycle

If  $\Delta i = 20\%(I_o)$ , then the output inductor will be:

$$L = 7\mu H$$

The Toko D124C series provides a range of inductors in different values, low profile suitable for large currents, 10 $\mu H$ , 5.3A is a good choice for this application. This will result to a ripple approximately 14% of output current.

### Feedback Compensation

The APU1855 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_o \times C_o}} \quad \text{---(7)}$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

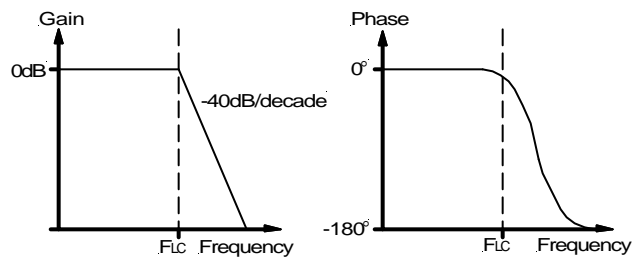


Figure 4 - Gain and phase of LC filter.



The APU1855's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_o} \quad \text{---(8)}$$

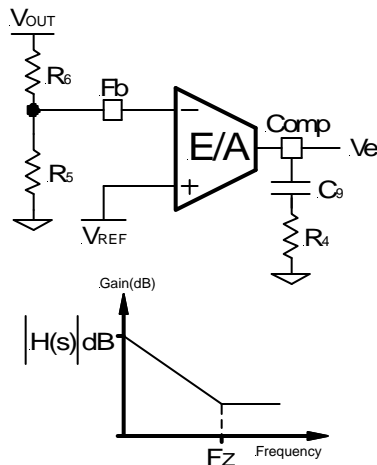


Figure 5 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function ( $V_e / V_{OUT}$ ) is given by:

$$H(s) = \left( g_m \times \frac{R_5}{R_6 + R_5} \right) \times \frac{1 + sR_4C_9}{sC_9} \quad \text{---(9)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \quad \text{---(10)}$$

$$F_z = \frac{1}{2\pi \times R_4 \times C_9} \quad \text{---(11)}$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency ( $F_o$ ):

$$F_o > F_{ESR} \text{ and } F_o \leq (1/5 \sim 1/10) \times f_s$$

Use the following equation to calculate  $R_4$ :

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{F_o \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \quad \text{---(12)}$$

Where:

$V_{IN}$  = Maximum Input Voltage

$V_{OSC}$  = Oscillator Ramp Voltage

$F_o$  = Crossover Frequency

$F_{ESR}$  = Zero Frequency of the Output Capacitor

$F_{LC}$  = Resonant Frequency of the Output Filter

$R_5$  and  $R_6$  = Resistor Dividers for Output Voltage Programming

$g_m$  = Error Amplifier Transconductance

For:

$V_{IN} = 5V$

$V_{OSC} = 1.25V$

$F_o = 30KHz$

$F_{ESR} = 26.52KHz$

$F_{LC} = 2.9KHz$

$R_5 = 1K$

$R_6 = 1.65K$

$g_m = 600\mu mho$

This results to  $R_4=104.4K\Omega$ . Choose  $R_4=105K\Omega$

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z \cong 75\%F_{LC}$$

$$F_z \cong 0.75 \times \frac{1}{2\pi \sqrt{L_o \times C_o}} \quad \text{---(13)}$$

For:

$L_o = 10\mu H$

$C_o = 300\mu F$

$F_z = 2.17KHz$

$R_4 = 86.6K\Omega$

Using equations (11) and (13) to calculate  $C_9$ , we get:

$C_9 = 698pF$

Choose  $C_9 = 680pF$

One more capacitor is sometimes added in parallel with  $C_9$  and  $R_4$ . This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_p = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor  $C_{POLE}$ :

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_s - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_s}$$

$$\text{for } F_P \ll \frac{f_s}{2}$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

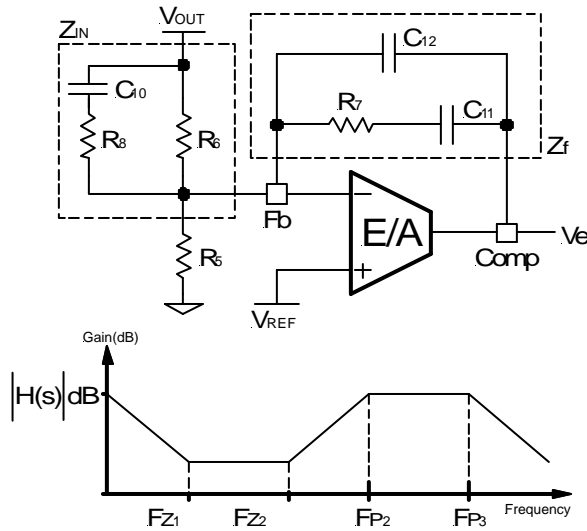


Figure 6 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f \gg 1 \quad \text{and} \quad g_m Z_{IN} \gg 1 \quad \text{---(14)}$$

By replacing  $Z_{IN}$  and  $Z_f$  according to Figure 7, the transfer function can be expressed as:

$$H(s) = \frac{1}{s R_6 (C_{12} + C_{11})} \times \frac{(1 + s R_7 C_{11}) \times [1 + s C_{10} (R_6 + R_8)]}{\left[ 1 + s R_7 \left( \frac{C_{12} \times C_{11}}{C_{12} + C_{11}} \right) \right] \times (1 + s R_8 C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left( \frac{C_{12} \times C_{11}}{C_{12} + C_{11}} \right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_o = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times L_o \times C_o} \quad \text{---(15)}$$

Where:

$V_{IN}$  = Maximum Input Voltage

$V_{OSC}$  = Oscillator Ramp Voltage

$L_o$  = Output Inductor

$C_o$  = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

- 1) Select the crossover frequency:  
 $F_o < F_{ESR}$  and  $F_o \leq (1/10 \sim 1/6) \times f_s$
- 2) Select  $R_7$ , so that  $R_7 \gg \frac{2}{g_m}$
- 3) Place first zero before LC's resonant frequency pole.  
 $F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

- 4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_s}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$$C_{12} > 50\text{pF}$$

If not, change  $R_7$  selection.



- 5) Place  $R_7$  in (15) and calculate  $C_{10}$ :

$$C_{10} \leq \frac{2\pi \times L_o \times F_o \times C_o}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

- 6) Place second pole at the ESR zero.

$$F_{P2} = F_{ESR}$$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if  $R_8 > \frac{1}{g_m}$

If  $R_8$  is too small, increase  $R_7$  and start from step 2.

- 7) Place second zero around the resonant frequency.

$$F_{Z2} = F_{LC}$$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

- 8) Use equation (1) to calculate  $R_5$ .

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than  $45^\circ$  for overall stability.

**TYPICAL PERFORMANCE CHARACTERISTICS**

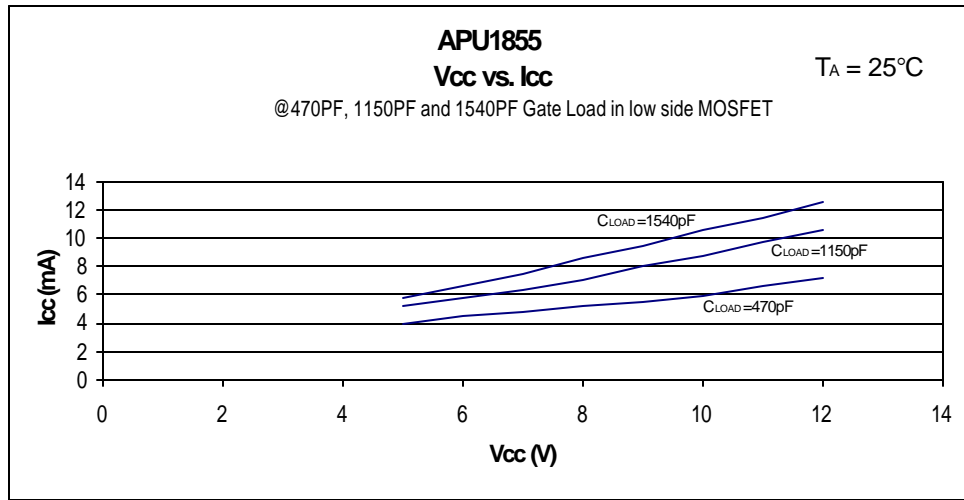


Figure 7 - Vcc vs. Icc

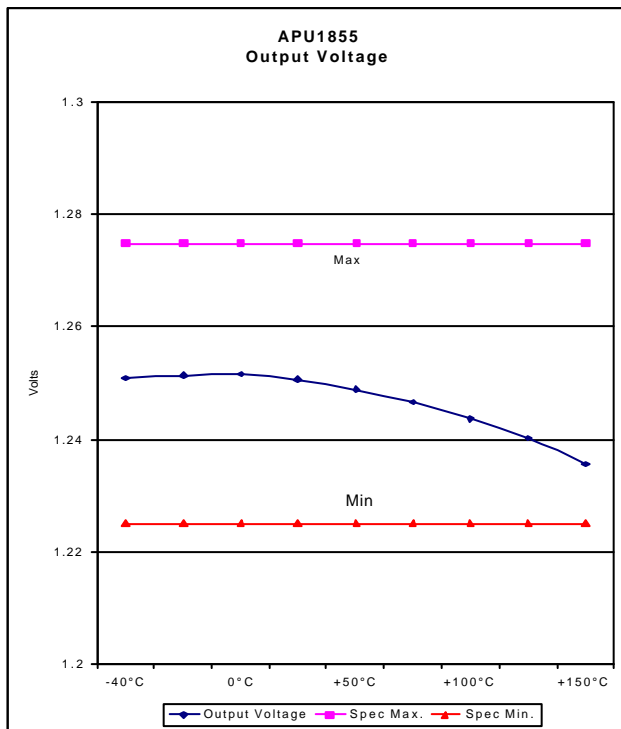


Figure 8 - Output Voltage

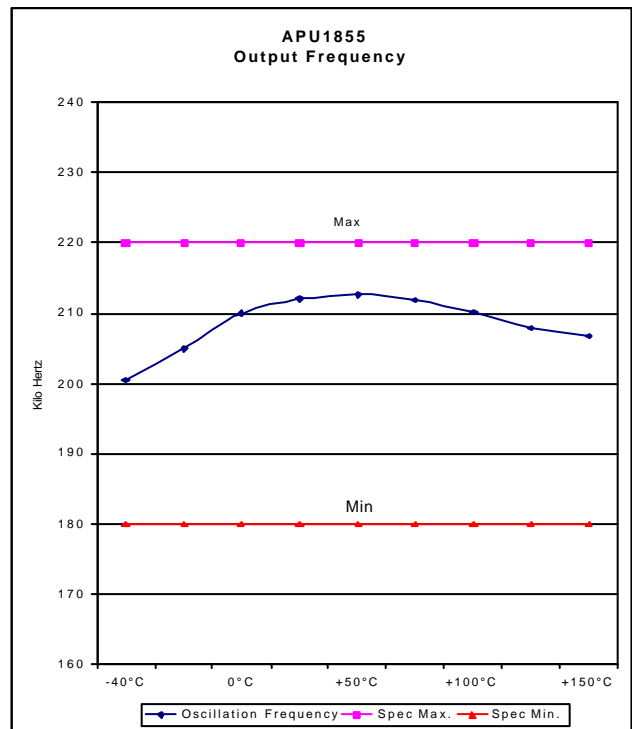


Figure 9 - Output Frequency



## TYPICAL PERFORMANCE CHARACTERISTICS

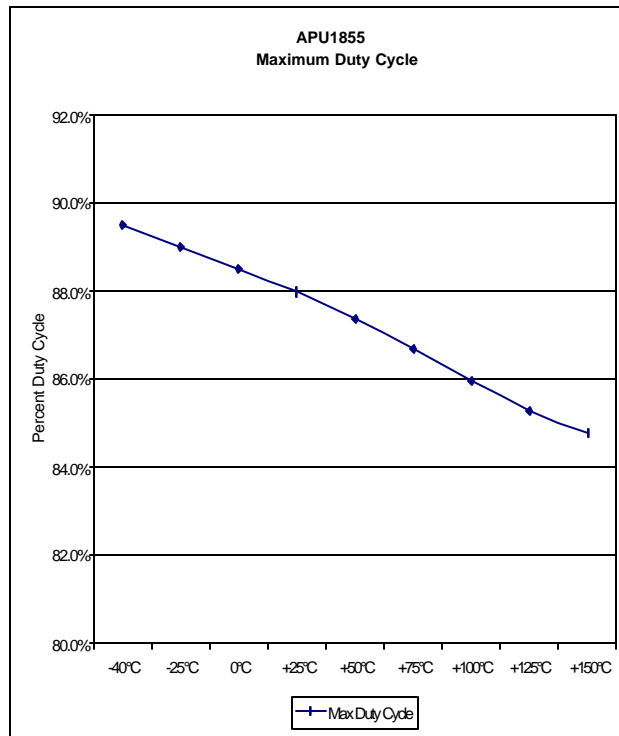


Figure 10 - Maximum Duty Cycle

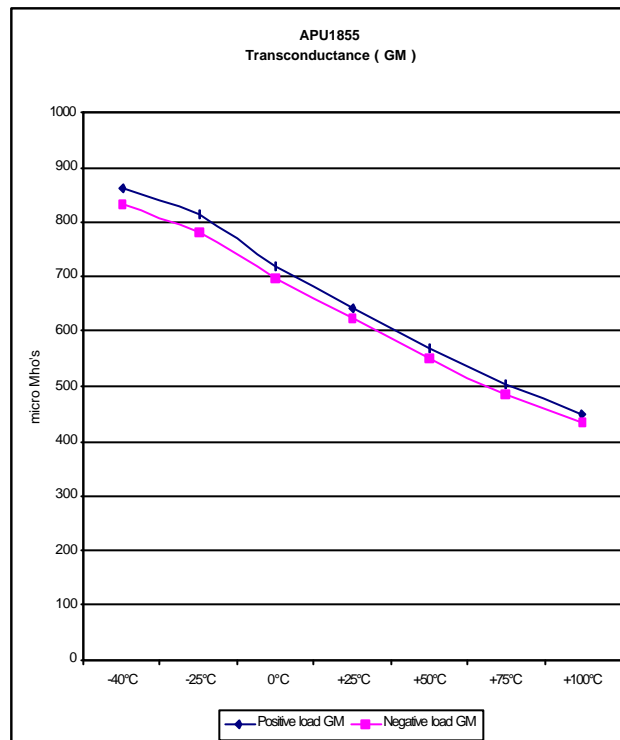


Figure 11 - Transconductance



TYPICAL APPLICATION

Single Supply 5V Input / Synchronous Converter

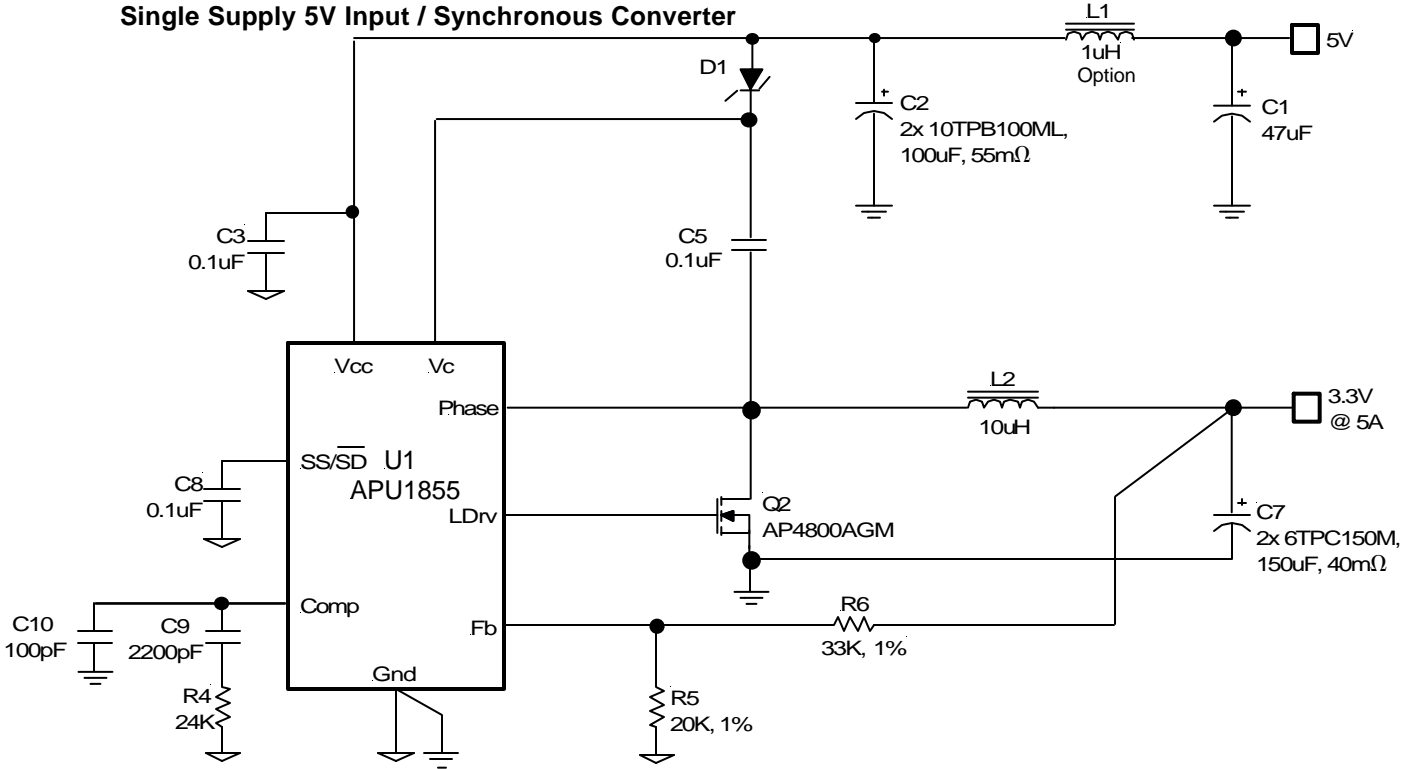


Figure 12 - Typical application of APU1855 in an on-board DC-DC converter using a single 5V supply.

Single Supply 5V Input / Asynchronous Converter

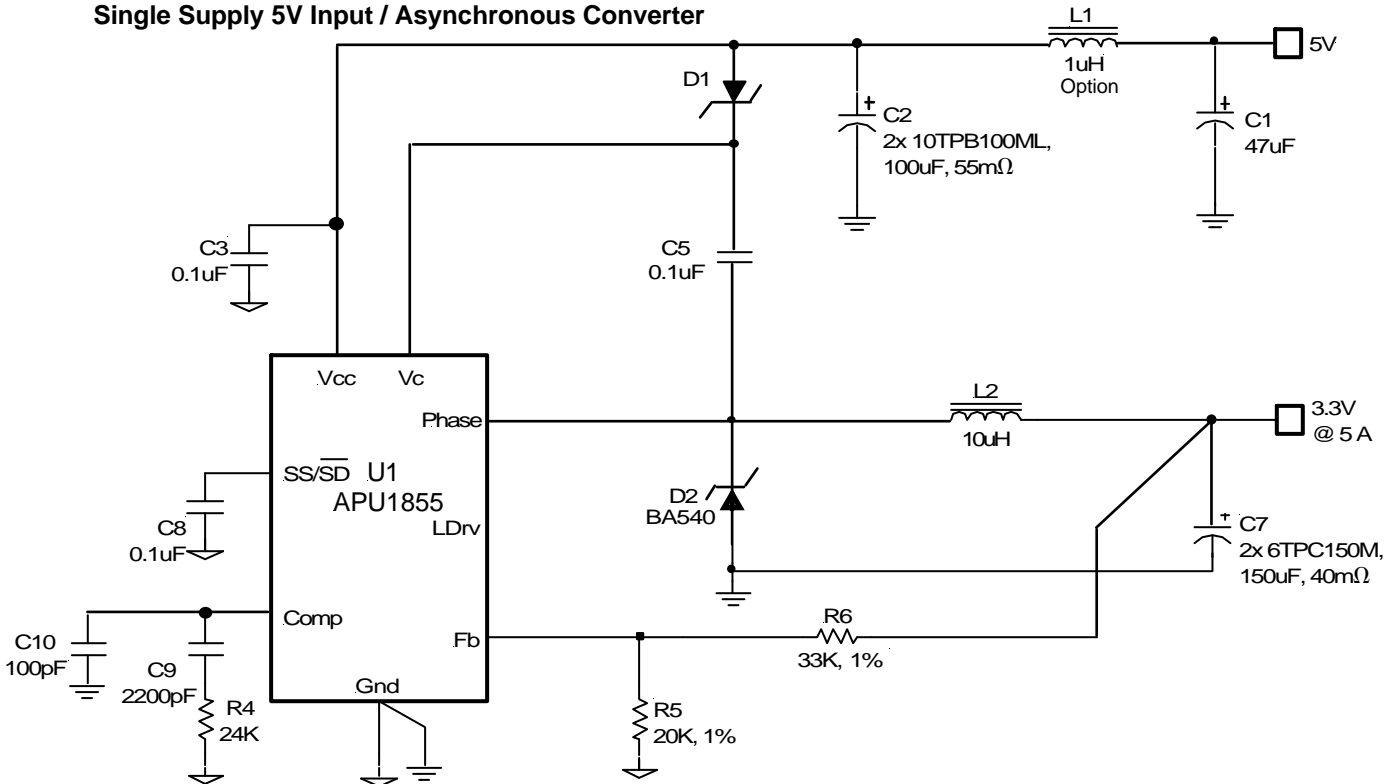


Figure 13 - Typical application of APU1855 in an on-board DC-DC converter using a single 5V supply.



### TYPICAL APPLICATION

Single Supply 12V Input / Synchronous Converter

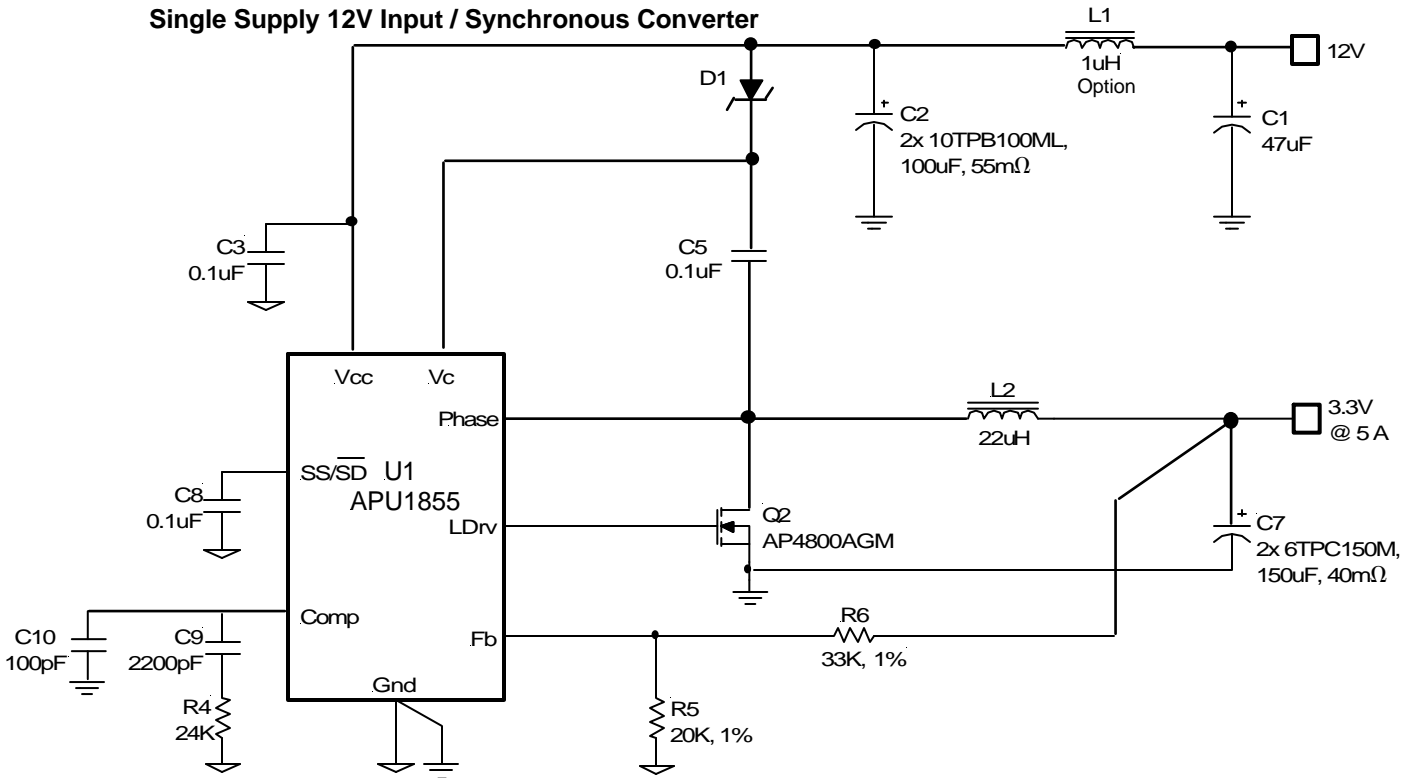


Figure 14 - Typical application of APU1855 in an on-board DC-DC converter using a single 12V supply.

Single Supply 12V Input / Asynchronous Converter

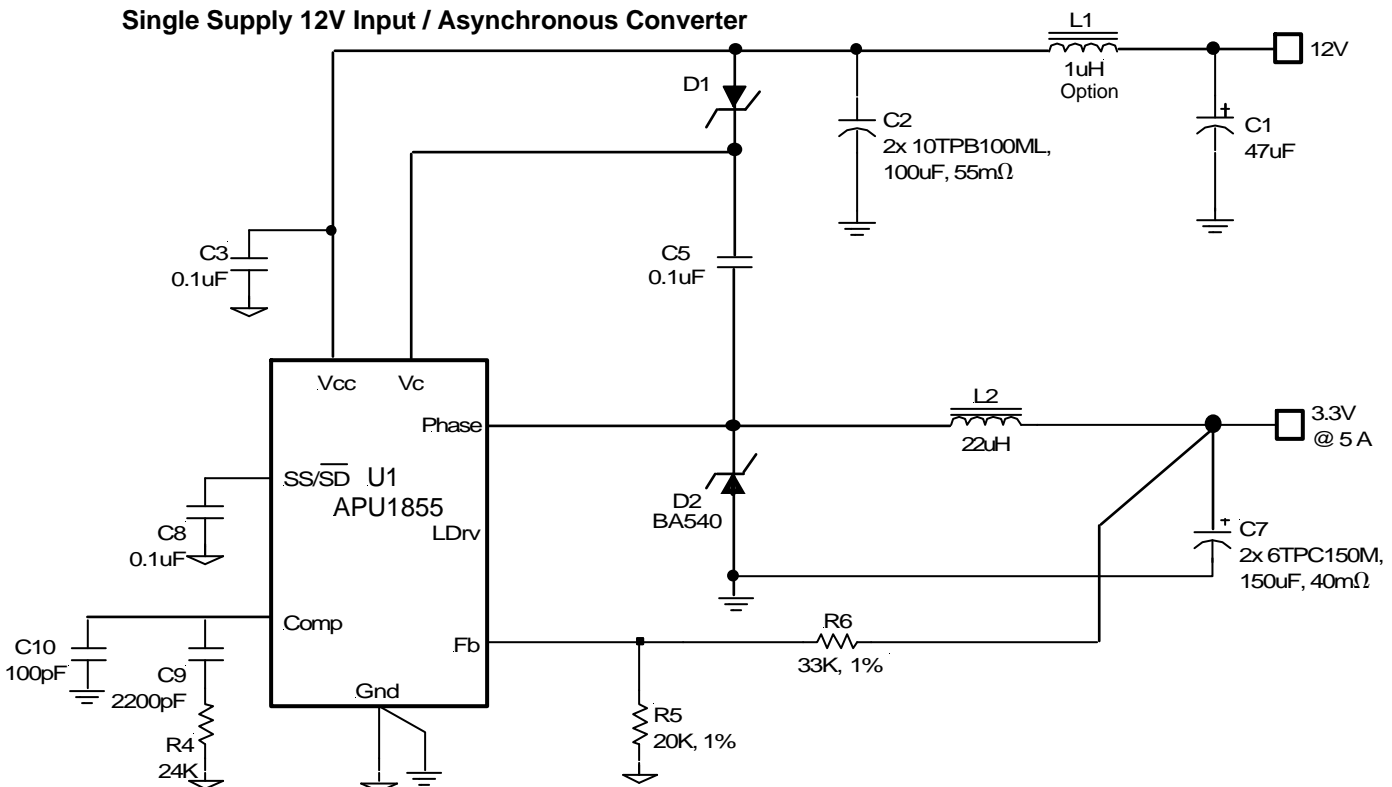


Figure 15 - Typical application of APU1855 in an on-board DC-DC converter using a single 12V supply.



## DEMO-BOARD WAVEFORMS

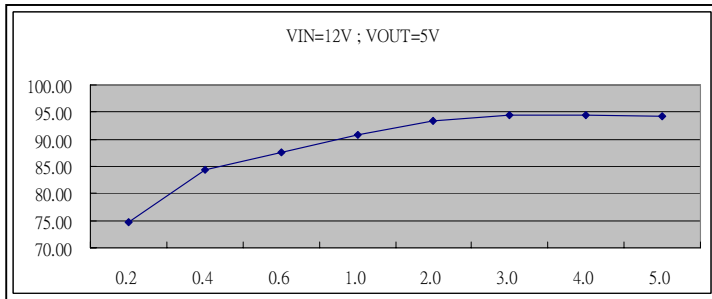


Figure 16 - Efficiency for APU1855 Evaluation Board.

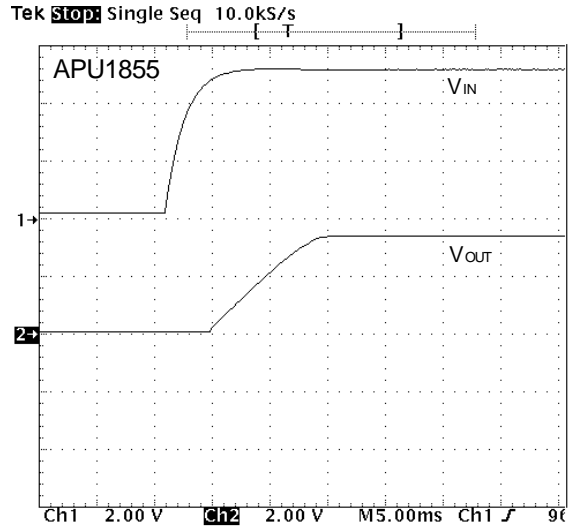


Figure 17 - Start-up time @ IOUT=5A.

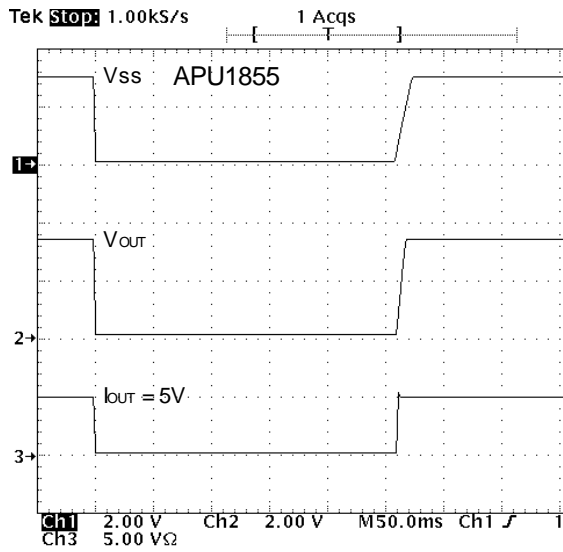


Figure 18 - Shutdown the output by pulling down the soft-start.

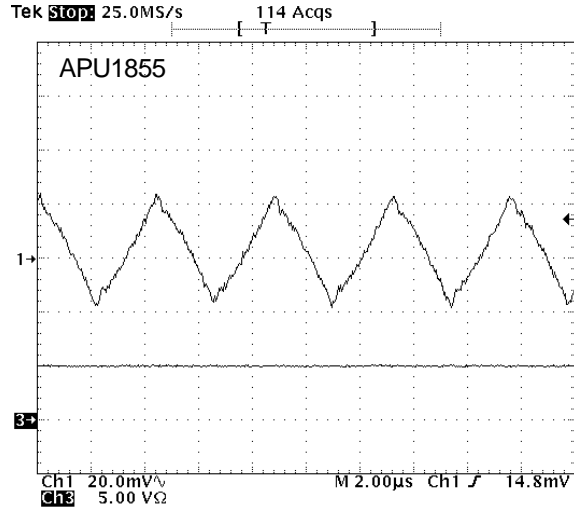


Figure 19 - 3.3V output voltage ripple @ IOUT=5A.

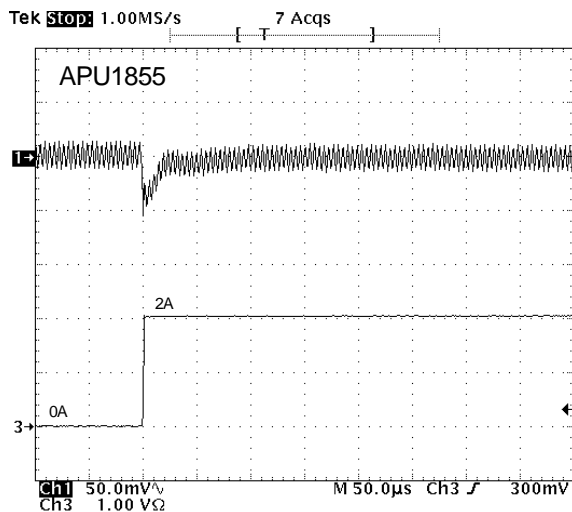


Figure 20 - Transient response @ IOUT = 0 to 2A.

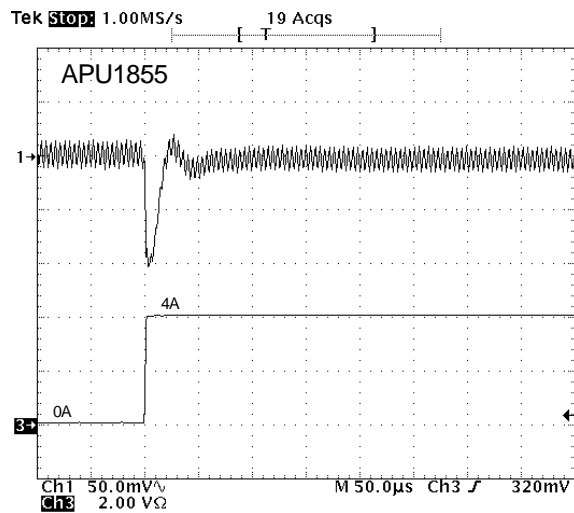


Figure 21 - Transient response @ IOUT = 0 to 4A.